

**DOCKET NO.: EIN-NL030433 (STNX01-30433)**

**PATENT**

**Customer No.: 84274**

In re application of : Raf Lodewijk Jan Roovers et al.

U.S. Serial No. : 10/552,816

Filed : October 11, 2005

For : PULSE DETECTION IN WIRELESS COMMUNICATION  
SYSTEM

Group No. : 2611

Examiner : Tanmay K. Shah

Confirmation No. : 5559



**MAIL STOP AF**

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Sir:

**PRE-APPEAL BRIEF REQUEST FOR REVIEW**

The Applicants respectfully request review of the final rejection in the above-identified application. No amendments are being filed with this request. This request is being filed with a notice of appeal. This review is requested for the reasons stated in the arguments below, demonstrating the clear legal and factual deficiency of the rejections of some or all of the claims.

Claims 1-12 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent Application Publication No. 2003/0224747 to Seema B. Anand ("*Anand*"). The Applicants respectfully traverses these rejections for the reasons set forth below.

Claim 1 recites a pulse detection unit, for detecting pulses in a received signal. The pulse detection unit includes a plurality of comparators; a sampling time generator, for generating signals indicative of a plurality of sampling time points; and a reference level generator, for generating a

plurality of reference levels. Claim 1 further recites that each of the comparators is programmable with a sampling time point selected from said plurality of sampling time points and with a reference level selected from said plurality of reference levels, and that the received signal is applied to each of the comparators such that each of the comparators produces a respective output signal based on a comparison between the received signal level and the selected reference level at the selected sampling time point.

The Applicants respectfully submit that the *Anand* reference does not anticipate the elements of the Applicants' invention. In particular, the *Anand* reference does not disclose a sampling time generator for generating signals indicative of a plurality of sampling time points. The final Office Action argues that *Anand* (Paragraph [0058]) teaches a sampling time generator for generating signals indicative of a plurality of sampling points. The final Office Action states "the charge pump feedback bias signal may be sampled."

*Anand* describes a phase-locked loop circuit including an array of selectable capacitors formed within the phase-locked loop circuit to enable the phase-locked loop circuit to provide a degree of coarse frequency control by adding or removing capacitors and a degree of fine frequency control by sinking or sourcing current from a charge pump into a loop filter. Further, *Anand* teaches that a finite state machine is provided within a voltage controlled oscillator calibration circuit that communicates with an external base-band processor to initiate a calibration process, and further to determine how many capacitors of an array of capacitors is formed within the phase-locked loop circuit should be coupled to provide the coarse frequency control. (*Anand*, Abstract).

*Anand*, however, fails to disclose "a sampling time generator, for generating signals indicative of a plurality of sampling time points; ....., wherein each of the comparators is

programmable with a sampling time point selected from said plurality of sampling time points ....., and wherein the received signal is applied to each of the comparators such that each of the comparators produces a respective output signal based on the comparison between the received signal level and the selected reference level at the selected sampling time point.” In particular, *Anand* does not teach a sampling time generator or any selected sampling time points because the voltage control oscillator (VCO) produces a signal having a frequency characteristic that is a function of an input voltage level of the VCO. (*Anand*, Paragraph [0009]).

In addition, the final Office Action cites *Anand*’s charge pump feedback bias (CPFB) signal to teach the generating signal(s) indicative of a plurality of sampling points. (February 13, 2009 Office Action, Page 5). However, the final Office Action also cites *Anand*’s charge pump feedback bias (CPFB) signal as the received signal. (February 13, 2009 Office Action, Pages 5-6). *Anand* does not disclose or teach that the CPFB signal is both the “generated signals indicative of a plurality of sampling points” and “a received signal applied to each of the comparators,” as recited in Applicants’ claims. Further, *Anand* does not describe “the received signal” as recited in independent Claim 1.

*Anand* provides a circuit that reduces the required gain level for the VCO and therefore reduces any introduced phase noise while accurately producing a signal with a specified frequency. (*Anand*, Paragraph [0010]). *Anand* (Paragraph [0058]) cited by the final Office Action merely describes the calibration circuit of the VCO. Moreover, the logic circuitry comprised by the finite state machine operates in the frequency domain. Thus the charge pump feedback bias signal cannot be interpreted as signals indicative of a plurality of sampling time points generated by a sampling time generator.

Accordingly, the Applicants respectfully request that the Examiner withdraw the § 102(b) rejection of Claim 1 and the rejections of the claims that depend from Claim 1.

The final Office Action asserts that the limitations of Claims 7-12 are similar to those found in Claims 1-6 and rejects Claims 7-12 based on the same rationale. Therefore, Claims 7-12 are allowable for at least the same, or similar, reasons as Claims 1-6, discussed above. Accordingly, the Applicants respectfully request withdrawal of the § 102(b) rejections of Claims 7-12.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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